

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: § Patent No.: 6,939,763 B2  
Till Schlösser et al. §  
§ Issued: September 6, 2005  
Serial No.: 10/720,730 §  
§ Group Art Unit: 2825  
Filed: November 24, 2003 §  
§ Examiner: Calvin Lee  
For: DRAM CELL ARRANGEMENT WITH VERTICAL MOS TRANSISTORS,  
AND METHOD FOR ITS FABRICATION

Certificate of Correction Branch  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Dear Sir:

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April 26, 2007	/Joseph M. Jong/
Date	Joseph M. Jong

REQUEST FOR CERTIFICATE OF CORRECTION

Attached is a Certificate of Correction for correcting several errors in the Claims section of the printed patent.

Applicants submit that the errors mentioned above were not by the applicants, but were made during the printing of the patent.

Respectfully submitted, and  
**S-signed pursuant to 37 CFR 1.4,**

/Joseph M. Jong, Reg. No. 42,698/

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**UNITED STATES PATENT AND TRADEMARK OFFICE**  
**CERTIFICATE OF CORRECTION**

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APPLICATION NO.: 10/720,730

ISSUE DATE: September 6, 2005

INVENTOR(S): Till Schlösser et al.

It is certified that errors appear in the above-identified patent  
and that said Letters Patent is hereby corrected as shown below:

In Claim 1, at Column 7, Line 1, replace "auxillary" with --auxiliary--.

In Claim 3, at Column 7, Line 28, replace "sourceldrain" with --source/drain--.

In Claim 11, at Column 8, Line 40, replace "Source/drain" with --source/drain--.

MAILING ADDRESS OF SENDER (Please do not use customer number below):

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